

DDR5 SO-DIMM series (Q2 2022)



Overview

ACES SO-DIMM series is designed for JEDEC memory modules for the latest data rate DDR5 and even has better performance. This interconnect solution provides high memory efficiency, high speed, and low voltages, which can help customers in consumers, networks, or Industrial fields with design advances in data signal integration.

Applications

- Meet high speed DDR5 requirement of JEDEC standards.
- 262pin, 4.00mm & 5.2mm height with standard and reverse configurations.
- Excellent mechanical structure with high density design of 0.50mm pitch.
- LCP housing with chemical and heat resistance withstands high temperature IR reflow.
- Compliance with MSDS & RoHS environmental requirement.

SO-DIMM Connector Family Status

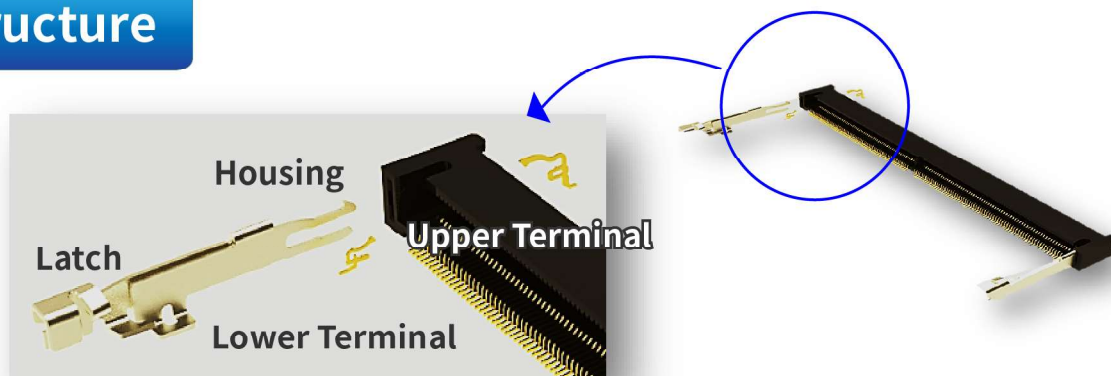
H 4.0mm

P/N	Description	Type	Circuits	Status
52746-262XX-XXX	0.5 mm pitch, D/R, R/A with 1u" Au plating	Standard	262	Available
52747-262XX-XXX	0.5 mm pitch, D/R, R/A with 1u" Au plating	Reverse	262	Available

H 5.2mm

P/N	Description	Type	Circuits	Status
52748-262XX-XXX	0.5 mm pitch, D/R, R/A with 1u" Au plating	Standard	262	Available
52749-262XX-XXX	0.5 mm pitch, D/R, R/A with 1u" Au plating	Reverse	262	Available

Structure



Specification

Rating	Current Rating	Voltage Rating	Operating Temperature Range	Operating Humidity Range
	0.5A/Per Pin	50V AC/DC	-40°C to 85°C	20 to 80%
Item		Specification		
Electrical	Contact resistance	40m Ω Max. per contact		
	Insulation resistance	500V DC/1 min 1M Ω Min.		
	Dielectric withstanding voltage	No discharge, flashover or breakdown. Current leakage: 1 mA max. (500V DC)		
Mechanical	Mating force	59.8N (Max.)		
	Durability	25 times		
	Vibration	No electrical discontinuity of 1 μ s or longer		
Environmental	Humidity	40°C, 90~95% RH, 96 hours		
	Temperature life	85°C for 96 hours		
	Salt Spray	8 hours		

SI Performance Specification

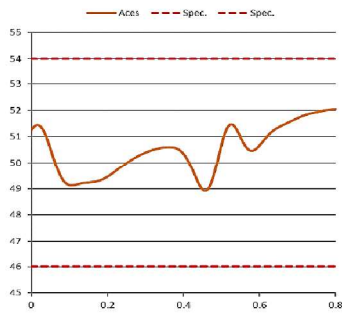
- Instrument: N5225B
- Sample: SO-DIMM 4H
- Frequency: 0.01~20GHz
- Calibration: 85056D
- De-embedding: AFR
- Date of measurement: 2021/12/20
- Specification: JEDEC JC-45.5
- Pre Simulation by Ansys HFSS



SI Performance

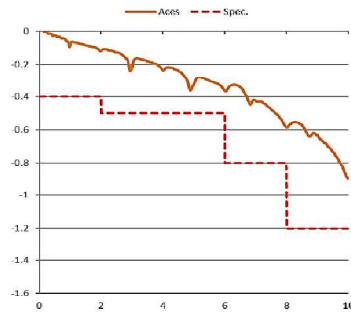


**Impedance
(80ps@10-90%)**

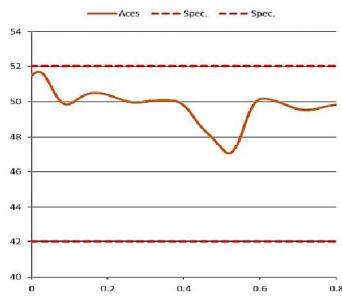
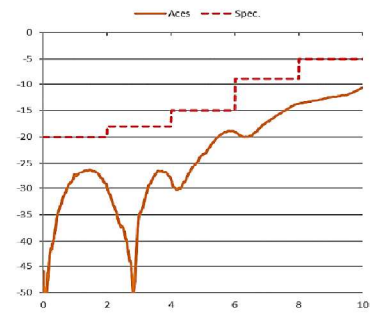


Upper
Contact

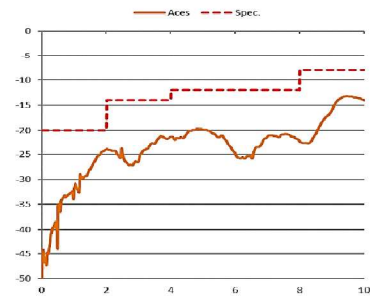
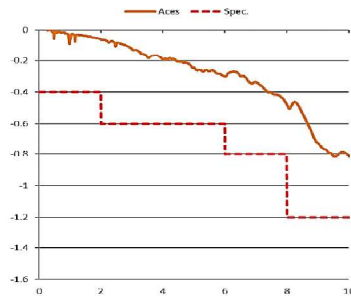
Insertion Loss



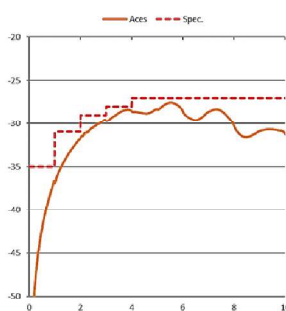
Return Loss



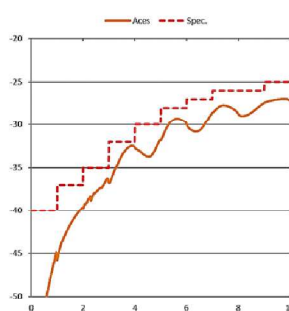
Lower
Contact



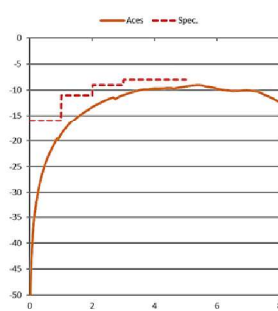
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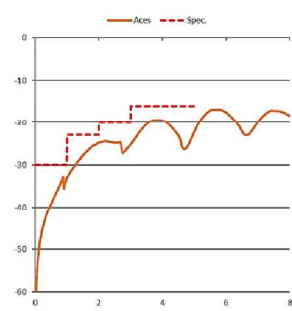
1:1 SAME FEXT



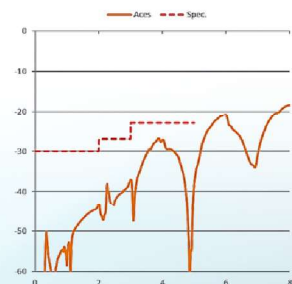
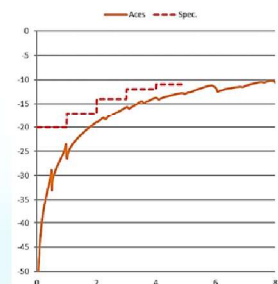
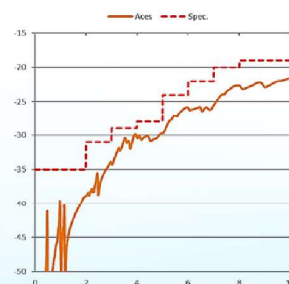
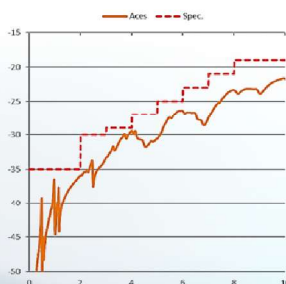
2:1 SAME NEXT



2:1 SAME FEXT



Upper
Contact

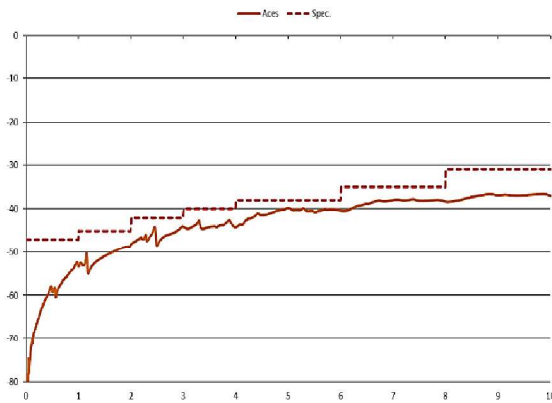


Lower
Contact

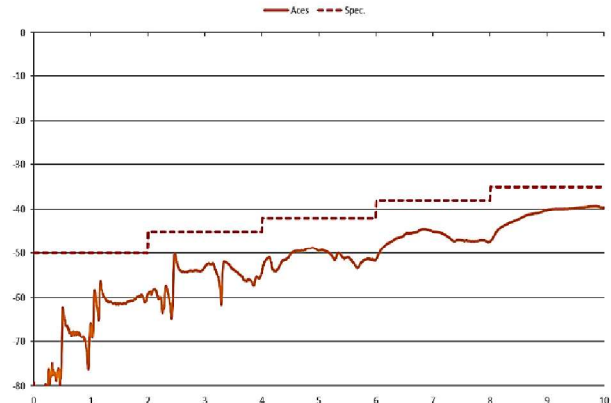
SI Performance



1:1 OPPOSITE NEXT



1:1 OPPOSITE FEXT

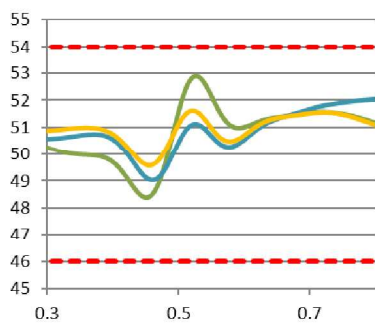


SI Performance (Comparison)

ACES — B — C — Spec.

Upper Contact

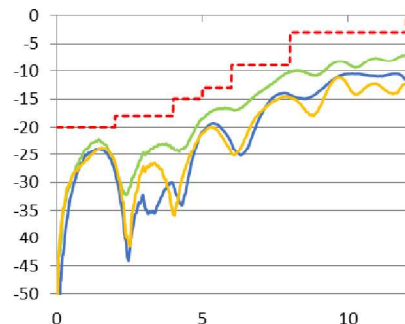
Impedance(80ps@10-90%)



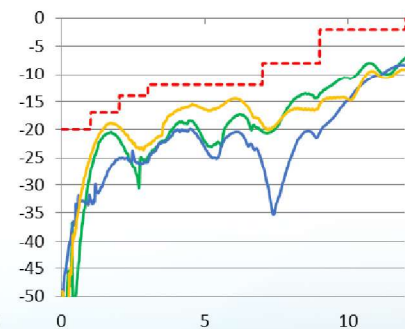
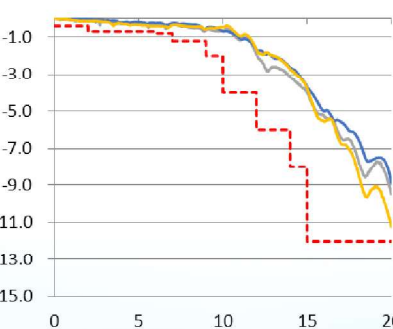
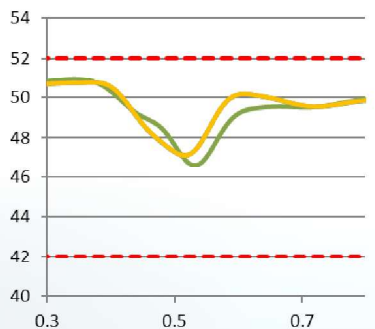
Insertion Loss



Return Loss

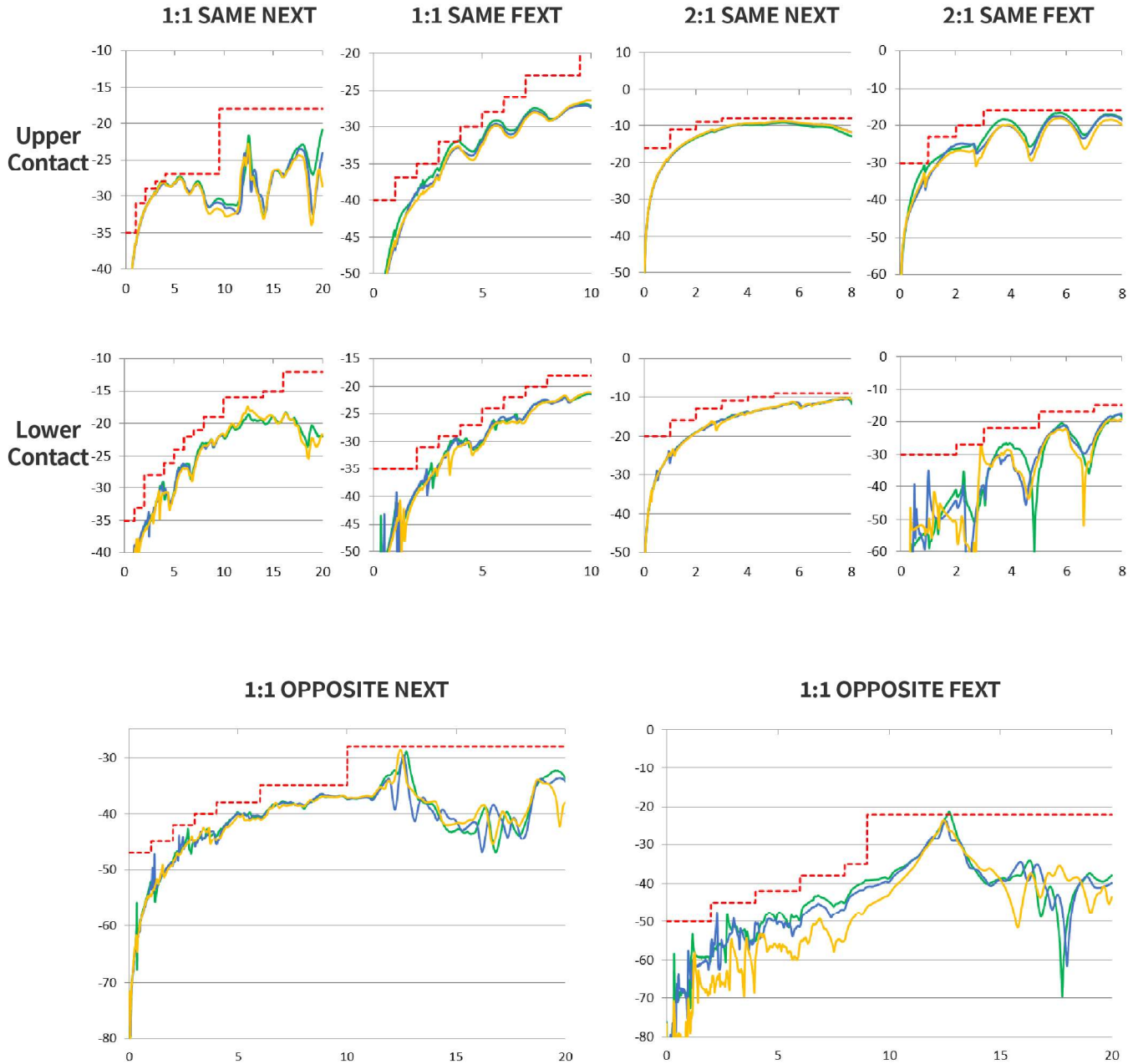


Lower Contact

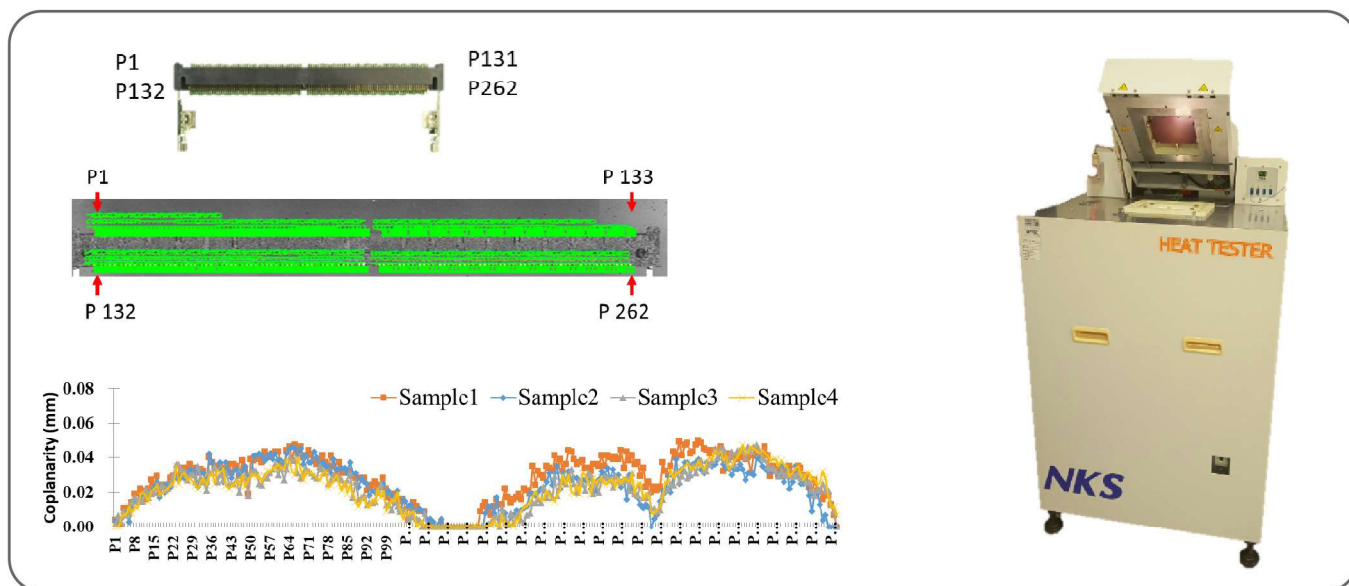


SI Performance (Comparison)

ACES — B — C — Spec.



IR Test for Coplanarity



Real object observation after IR, after peak 260°C, Coplanarity 0.05 Max.

Drop Testing

Mode: height 1M, one corner, three edges, and six-sided drops

Specification: a. Apparent(Latch, dummy card without detached)

b. Dummy card without detached

c. 40m Ω Max.(initial) per contact

Δ 10m Ω Max.(finish) (refer to JEDEC March 2021)

Result:

Specification	Sample	1	2	3	4
Appearance	Housing Damaged	No	No	No	No
	Latch Deformed	No	No	No	No
	Card Operation	Normal	Normal	Normal	Normal
Dummy Card	Detached	No	No	No	No
Initial Impedance 28~33 m Ω – Pass Finish Impedance 28~35 m Ω – Pass					